

# Laboratory report

Central Application Laboratory

C.A.B. - Elcoma

Eindhoven - the Netherlands

No : ETT 8603

Title : Stability analysis of the receiving amplifier  
of the TEA 1060/61

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Nederlandse Philips Bedrijven N.P.B. Eindhoven - Nederland



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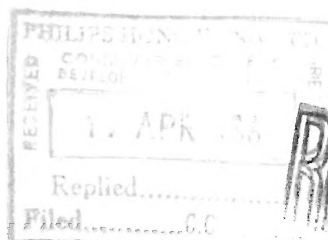


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title STABILITY ANALYSIS OF THE RECEIVING AMPLIFIER OF THE TEA1060/61

author P.J.M. Sijbers

### ABSTRACT

A brief stability-analysis is given concerning the receiving amplifier of the speech/transmission circuits TEA1060/61. Both resistive and capacitive loads are considered.

It is shown that 2 small external capacitors are necessary to guarantee stability. Furthermore with a capacitive load an extra series resistor must be used for stable operation.

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Appr. J.J. van der Kam

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STABILITY ANALYSIS OF THE RECEIVING AMPLIFIER OF THE TEA1060/611. INTRODUCTION

A brief analysis of the stability of the receiving amplifier of the electronic speech-transmission circuits TEA1060/61 is given. Gain and phase plots of the product of the forward gain and the feedback factor are used for this purpose.

Two cases are considered:

- normal application with a resistive load (dynamic earpiece)
- application with a capacitive load (Piezo earpiece)

2. PRINCIPLE OF THE RECEIVING AMPLIFIER

Fig.1 shows the simplified circuit diagram of the receiving amplifier.

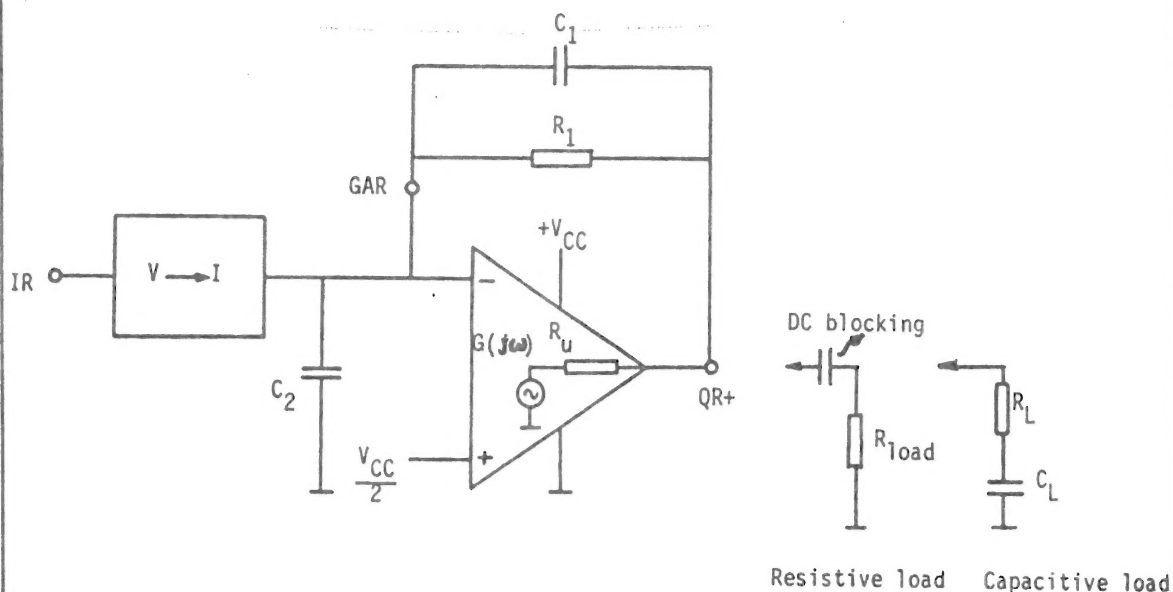


Fig.1 Receiving amplifier of the TEA1060/61.  
The complementary output is not shown.

The opamp  $G(j\omega)$  is used as a current to voltage converter with 100% feedback. It contains a class-B output stage.

A complementary receiving output is obtained by an inverter equipped with a second class-B output stage.

Stability of the part with 100% feedback is considered.

Only asymmetrical loads are used in the calculations.

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The open loop gain of the opamp  $G(j\omega)$  is shown in Fig. 2

$$\text{Open loop gain } G(j\omega) = \frac{G_o}{(1+j\omega\tau_1)(1+j\omega\tau_2)} \cdot \frac{R_{load}}{R_{load} + R_u}$$

in which  $G_o = 60 \text{ dB}$  DC open loop gain

$1/(2\pi\tau_1) = 9 \text{ kHz}$  First pole frequency

$1/(2\pi\tau_2) = 4 \text{ MHz}$  Second pole frequency

$R_u = kT/qI$  Output resistance of the class-B output stage

In case the output stage is not driven

$R_u = 420 \text{ Ohm}$  ( $I = 60 \mu\text{A}$  quiescent current of the output stage)

$$\text{Feedback factor } k(j\omega) = \frac{1+j\omega R_1 C_1}{1+j\omega R_1 (C_1 + C_2)}$$

### 3. STABILITY WITH RESISTIVE LOAD

A resistive load connected to the earpiece output will decrease the open loop gain. This means that the most unfavourable situation concerning stability occurs when the output is unloaded. Assume  $R_{load}$  is infinite,  $C_1 = 0$  and  $C_2 = 4 \text{ pF}$  (parasitic capacitance).

$$\text{This results in a feedback factor } k(j\omega) = \frac{1}{1+j\omega R_1 C_2}$$

Now a third pole ( $\omega = 1/R_1 C_2$ ) is introduced in the loop gain  $G(j\omega) \cdot k(j\omega)$ .

Fig. 3 shows  $|G(j\omega)|$  and  $|1/k(j\omega)|$  and the phase of  $G(j\omega) \cdot k(j\omega)$ . It can be seen very easily that the circuit is unstable. The phase margin at  $1.8 \text{ MHz}$  ( $|G(j\omega) \cdot k(j\omega)| = 0 \text{ dB}$ ) is negative ( $-10$  degrees). For this reason, external capacitors  $C_1$  and  $C_2$  are introduced in the normal application, resulting in a reduced feedback factor in order to increase the phase margin. Additionally capacitor  $C_1$  determines together with  $R_1$  the cut-off frequency for the normal straightforward gain. Capacitor  $C_2$  has no influence on the normal straightforward gain.

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Fig. 4 shows that stability can easily be guaranteed with  $C_1 = 100$  pF and  $C_2 = 1$  nF. Phase margin in this case is about 80 degrees.

In case  $C_1$  is changed in order to obtain a different cut-off frequency, the value of  $C_2$  must be kept at  $C_2 = 10.C_1$ .

#### 4. STABILITY WITH A CAPACITIVE LOAD

Fig. 1 also shows the receiving amplifier with a capacitive load connected to the earpiece output (e.g. a Piezo transducer). A 50 nF symmetrical load can be seen as a 100 nF single ended load for both output stages.

An extra pole  $\omega = 1/(R_u C_L)$  is now introduced in the formula for the open loop gain.

$$G'(j\omega) = G(j\omega) \frac{1}{1+j\omega R_u C_L} = \frac{G_o}{(1+j\omega\tau_1)(1+j\omega\tau_2)(1+j\omega R_u C_L)}$$

Fig. 5 shows  $|G'(j\omega)|$  and  $|1/k(j\omega)|$  together with the phase of  $G'(j\omega).k(j\omega)$ .

It is obvious that the system will be instable. Phase margin is zero.

A resistor in series with the capacitive load will produce a zero  $\omega = 1/(R_L C_L)$  in the formula for the open loop gain.

$$G''(j\omega) = \frac{G_o}{(1+j\omega\tau_1)(1+j\omega\tau_2)} \cdot \frac{1+j\omega R_L C_L}{1+j\omega(R_u+R_L)C_L}$$

Fig. 6 shows the gain and phase plots with  $R_L = 25$  Ohm. This results in a phase margin of about 45 degrees.

Fig. 7 gives the result with  $R_L = 50$  Ohm. Phase margin is about 70 degrees in this case.

When a symmetrical capacitive load is used, both output stages need a resistor in series with the capacitive load to guarantee stability. This means that a 50 nF symmetrical load needs a 50 Ohm series resistor for 45 degrees phase margin. With a 100 Ohm series resistor the phase margin will be about 70 degrees.

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## 5. CONCLUSION

The receiving amplifier of the TEA1060/61 needs two small capacitors to guarantee stability when resistive loads are applied. One of these capacitors is also used to adjust the upper cut-off frequency. In case of a capacitive load, a resistor in series with the capacitive load must be used to maintain stability.

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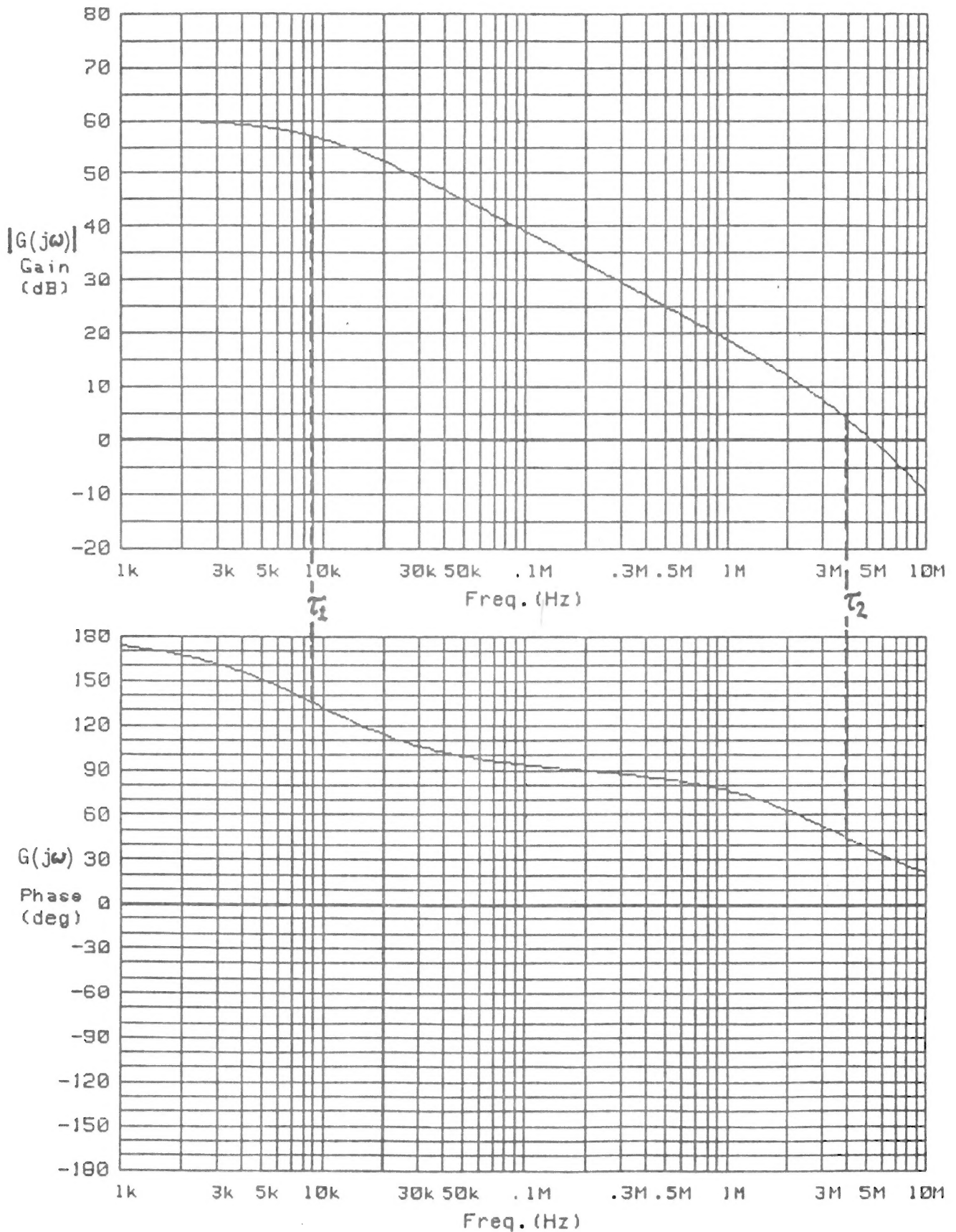
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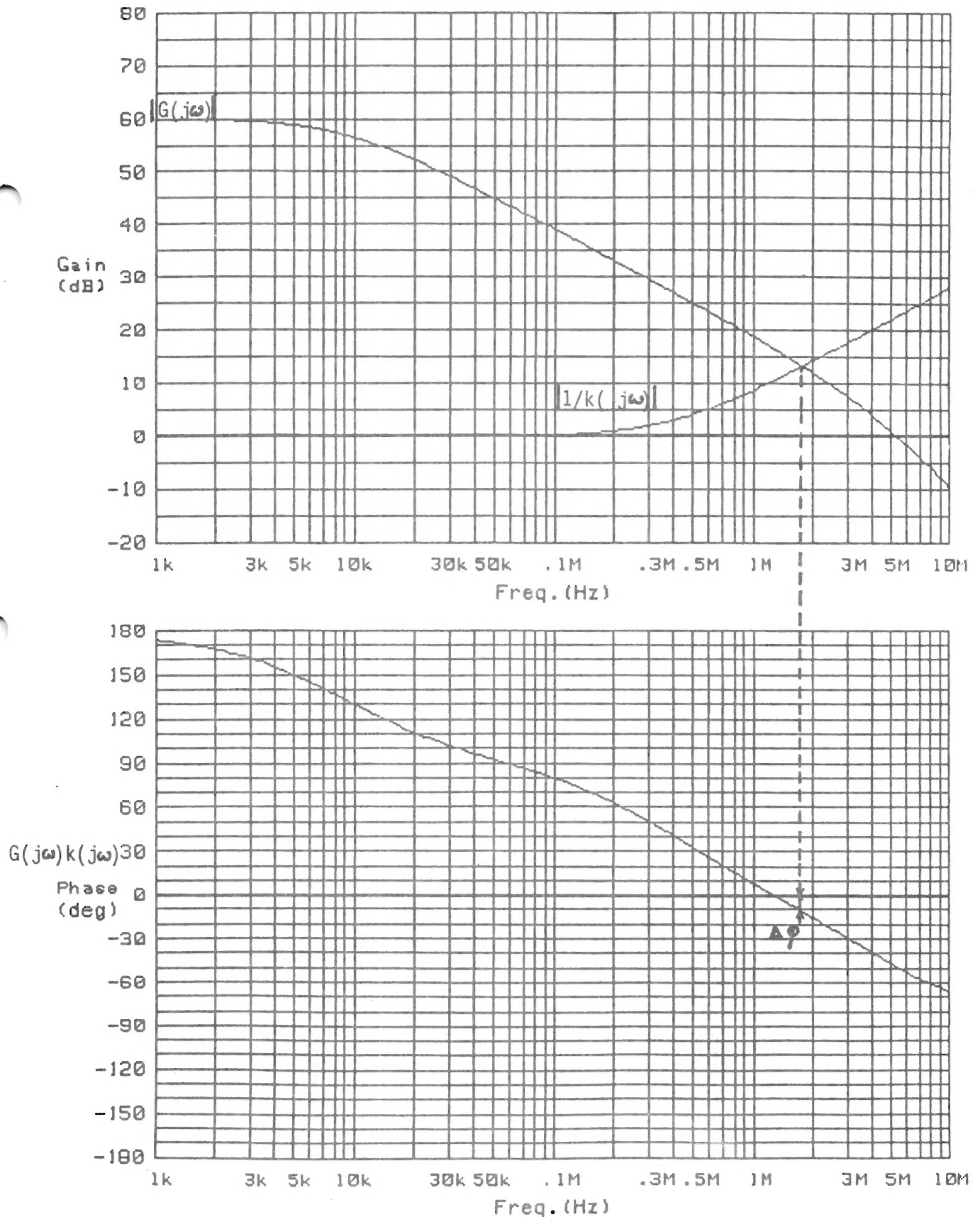
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$G_0 = 60 \text{ dB}$   
 $F_{p1} = 9000 \text{ Hz}$   
 $F_{p2} = 4000 \text{ kHz}$   
 $CL = 0 \text{ nF}$   
 $RL = 0 \text{ Ohm}$   
 $R_u = 420 \text{ Ohm}$   
 $R_1 = 100 \text{ kOhm}$   
 $C_1 = 0 \text{ pF}$   
 $C_2 = 0 \text{ pF}$

Fig.2 Open loop gain  $G(j\omega)$ 

$G_0 = 60$  dB  
 $F_{p1} = 9000$  Hz  
 $F_{p2} = 4000$  kHz  
 $CL = 0$  nF  
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 $R_u = 420$  Ohm  
 $R_1 = 100$  kOhm  
 $C_1 = 0$  pF  
 $C_2 = 4$  pF

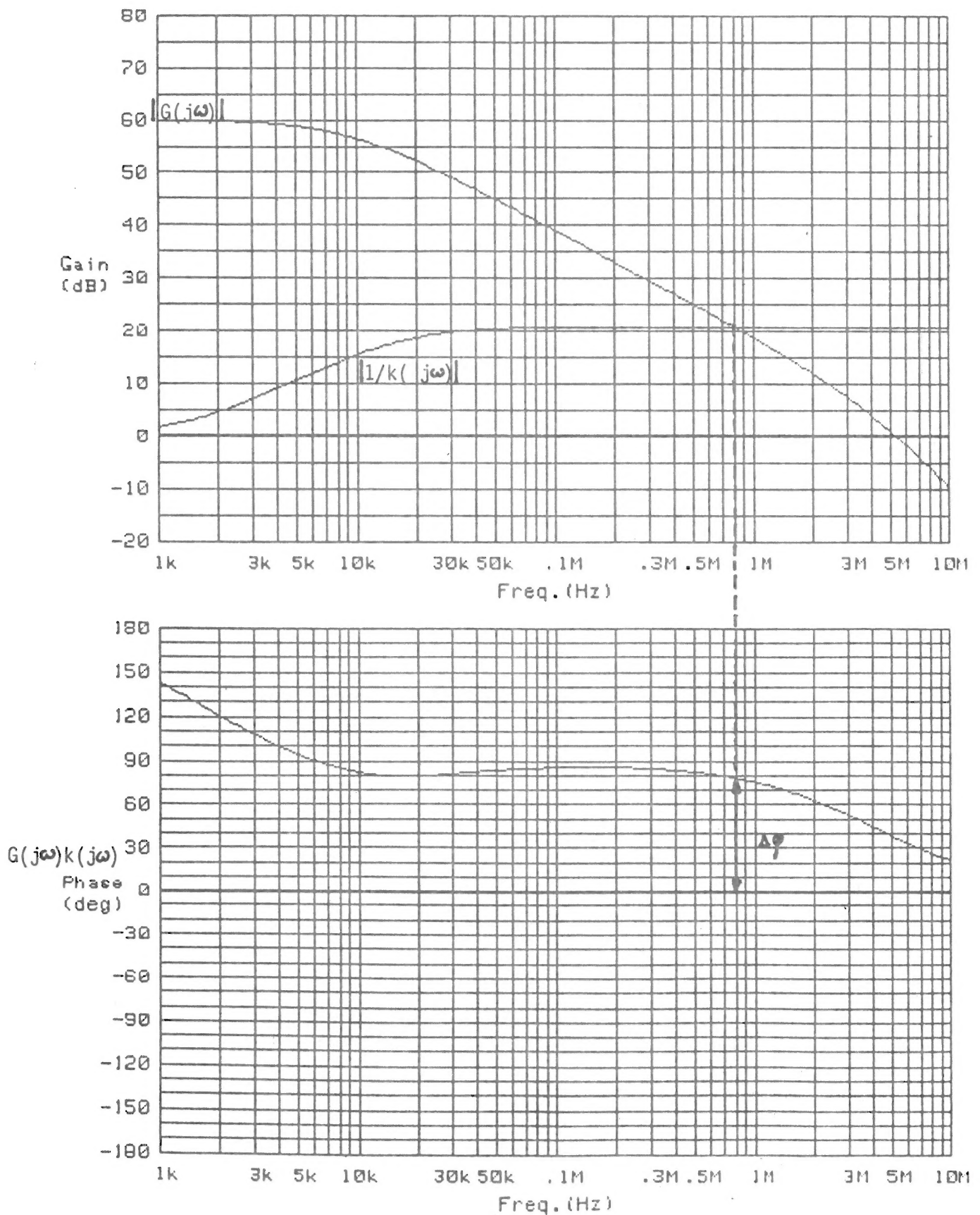
Fig.3 Gain and phase plots with resistive load.  
without stability capacitors.





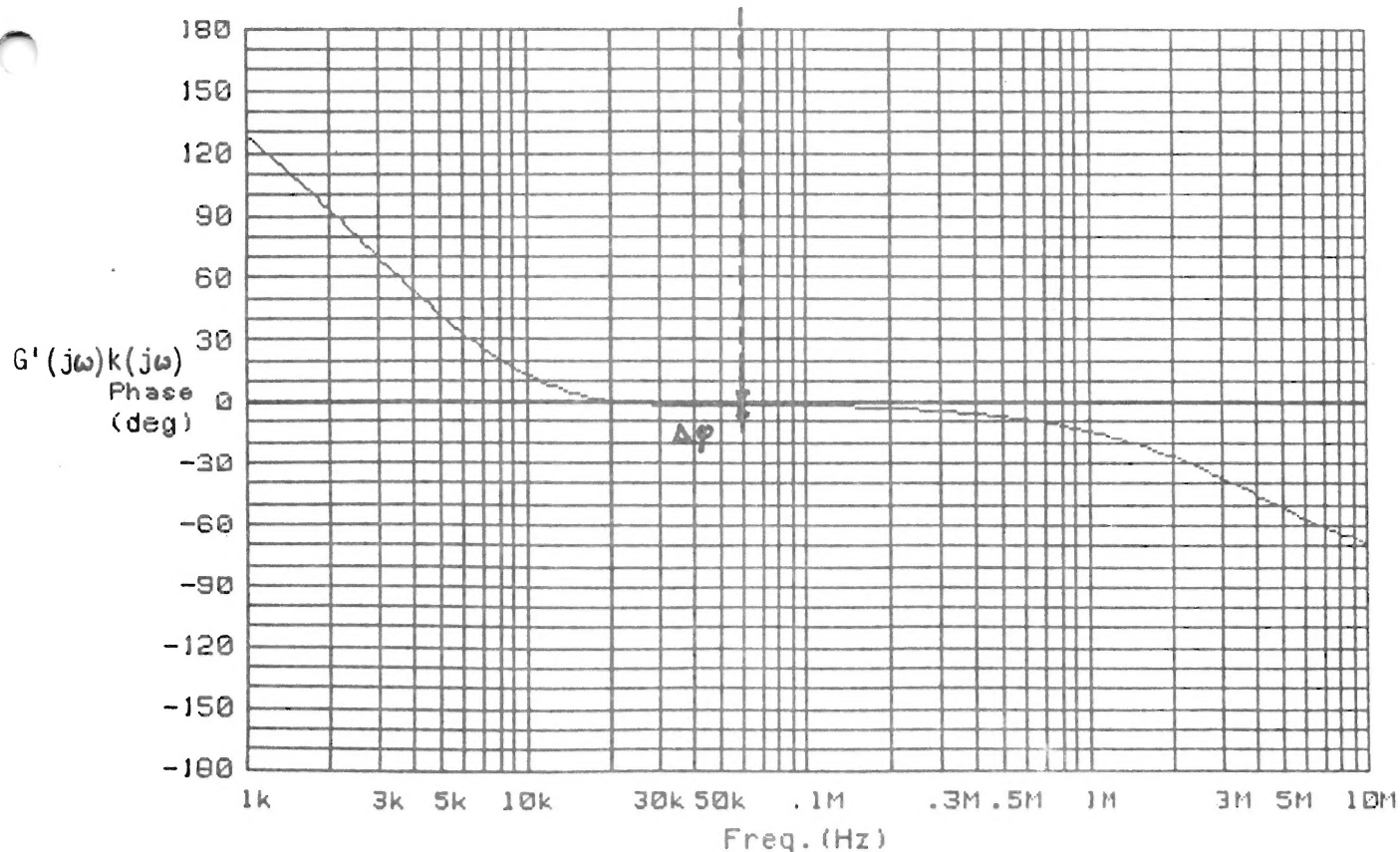
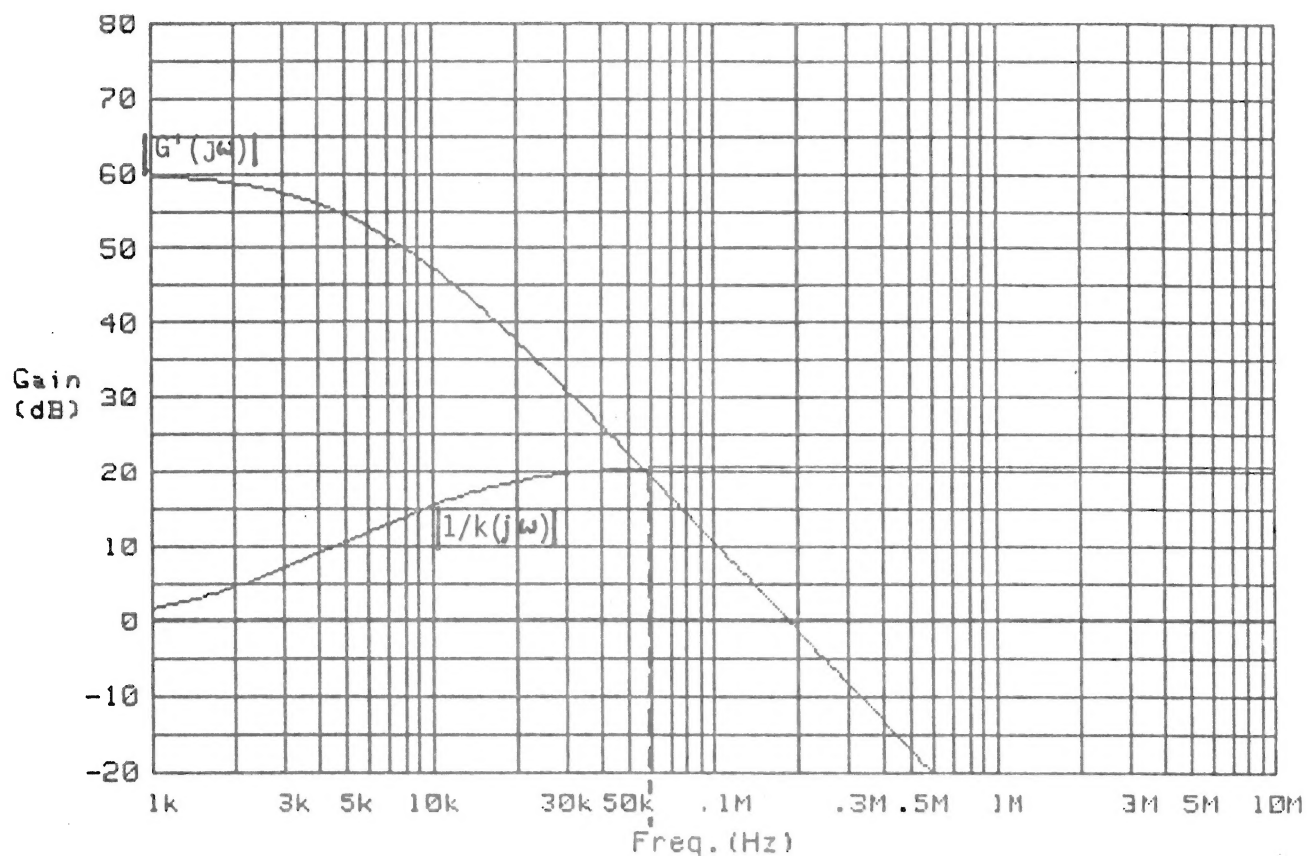
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 $R_u = 420$  Ohm  
 $R_1 = 100$  kOhm  
 $C_1 = 100$  pF  
 $C_2 = 1$  nF

Fig.4 Gain and phase plots with resistive load with stability capacitors.



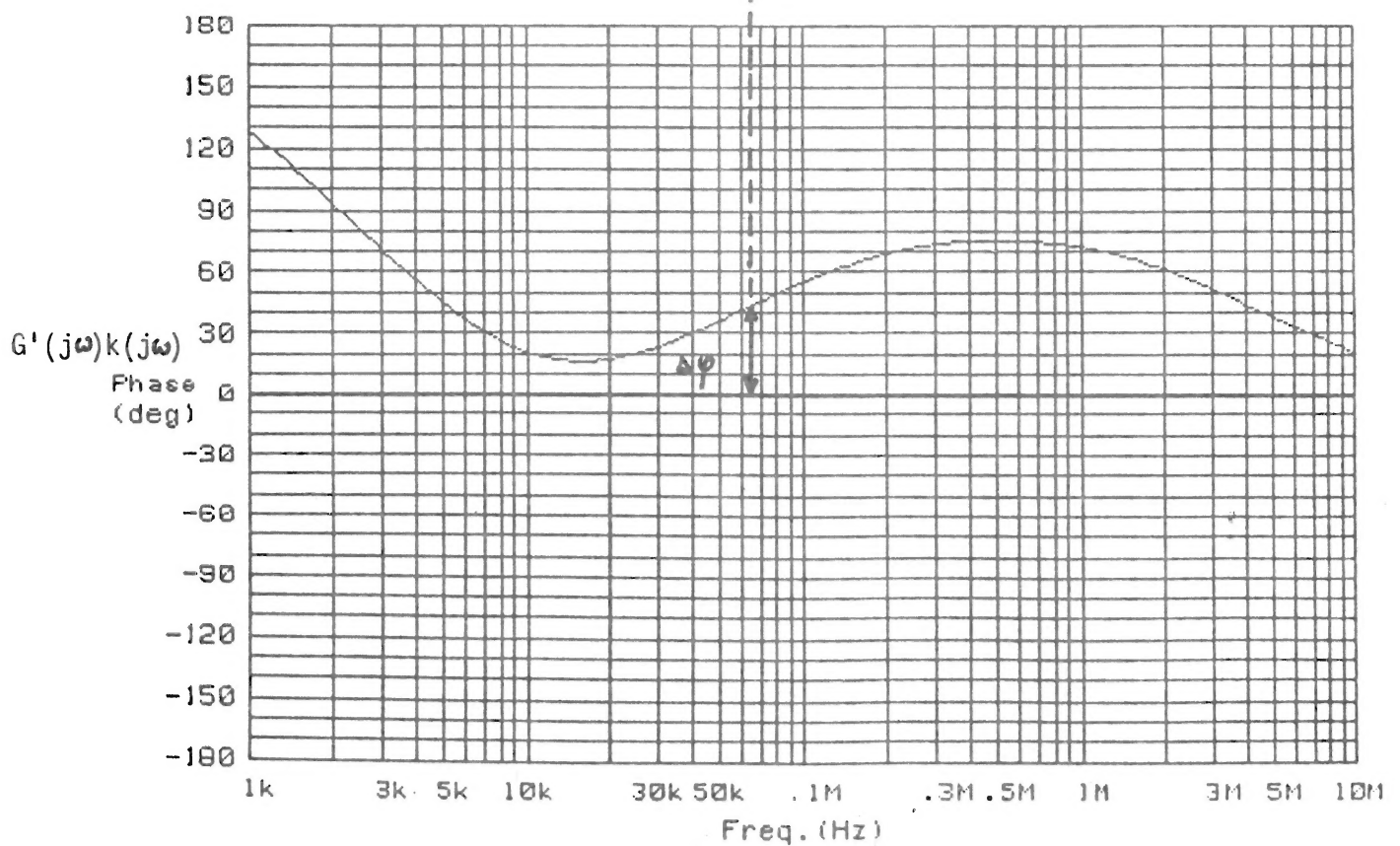
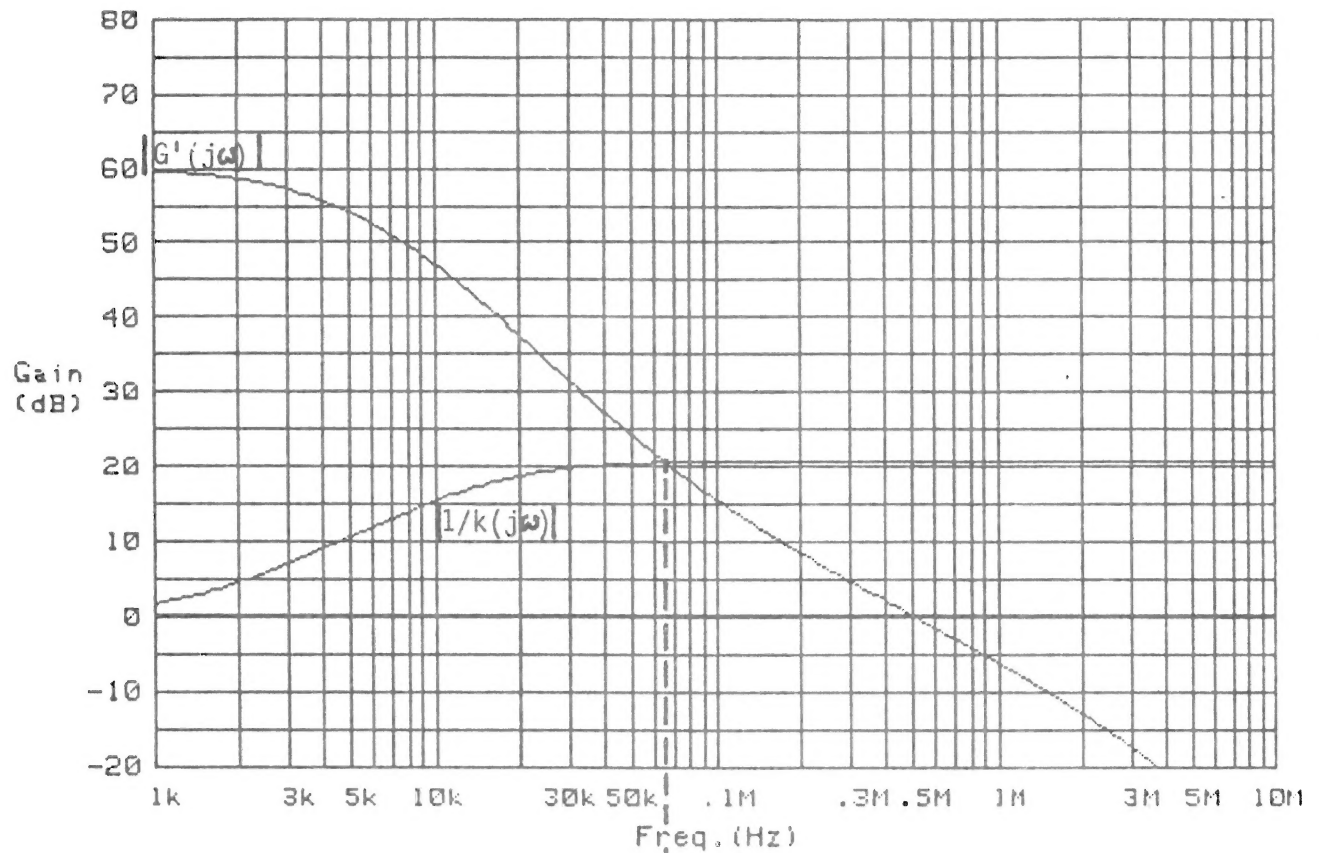
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 $C_2 = 1 \text{ nF}$

Fig.5 Gain and phase plots with capacitive load (100nF) without series resistor.



$G_0 = 60 \text{ dB}$   
 $F_{p1} = 9000 \text{ Hz}$   
 $F_{p2} = 4000 \text{ kHz}$   
 $CL = 100 \text{ nF}$   
 $RL = 25 \text{ Ohm}$   
 $R_u = 420 \text{ Ohm}$   
 $R_1 = 100 \text{ kOhm}$   
 $C_1 = 100 \text{ pF}$   
 $C_2 = 1 \text{ nF}$

Fig.6 Gain and phase plots with capacitive load (100nF)  
with 25 Ohm series resistor





$G_0 = 60 \text{ dB}$   
 $F_{p1} = 9000 \text{ Hz}$   
 $F_{p2} = 4000 \text{ kHz}$   
 $C_L = 100 \text{ nF}$   
 $R_L = 50 \text{ Ohm}$   
 $R_u = 420 \text{ Ohm}$   
 $R_1 = 100 \text{ kOhm}$   
 $C_1 = 100 \text{ pF}$   
 $C_2 = 1 \text{ nF}$

Fig.7 Gain and phase plots with capacitive load (100nF) and 50 Ohm series resistor.

